# Measuring the thermal conductivity of the GaN buffer layer in AlGaN/GaN HEMTs

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The thermal conductivity of the GaN buffer layer in AlGaN/GaN devices can be determined by measuring the vertical temperature gradient through this layer. In this work, diamond micro-thermometers and standard micro-Raman thermography were used to determine the surface and volumetric depth average temperature respectively of the carbon-doped GaN buffer layer in AlGaN/GaN transistors. By comparing measured temperatures with finite element thermal simulation, a thermal conductivity of 200±20 $Wm^{-1}K^{-1}$ was obtained for a carbon-doped GaN layer with a doping concentration of $10^{17}$ $cm^{-3}$.



**1 Introduction** AlGaN/GaN high electron mobility transistors (HEMTs) are excellent candidates for high frequency [1] and high power [2] applications. During operation, a temperature rise in the active GaN region of the device has a significant effect on device reliability and performance. Considering an AlGaN/GaN transistor comprising an AlGaN barrier layer, a GaN buffer layer and an AlN nucleation layer grown on a SiC or other substrate, the temperature rise in the device channel has three main determining factors; the thermal conductivity of the GaN layer, the thermal boundary resistance of, for example, the AlN nucleation layer (or of strain relief layers for devices fabricated on Si substrates) and the thermal conductivity of the substrate. The thermal conductivity of the GaN layer in such devices is generally assumed to be 160 $Wm^{-1}K^{-1}$ [3,4], when thermal modelling is applied to determine the peak channel temperature. However, there is little experimental validation on the actual thermal conductivity of transistor epitaxial GaN layers which may be dependent on the dopants used and their concentrations such as, for example, carbon (C) doping [5] for power transistors or iron (Fe) doping [6] for microwave transistors. The temperature averaged volumetrically through the GaN layer in HEMTs can be determined by the micro-Raman thermography technique [4]. However, additional information about the vertical temperature gradient within the GaN layer would be beneficial for verifying device thermal models and in particular, verifying the GaN layer thermal conductivity, as this strongly influences the peak channel temperature. This can be gained by measuring the temperature at the device surface in addition to the average temperature through the GaN buffer layer. Photoluminescence spectroscopy can be utilised to measure the surface temperature of an AlGaN/GaN device channel using the temperature

dependence of the GaN band edge peak but the measurement is significantly affected by thermal and piezoelectric stress in the GaN layer [7]. Simon et al. [8] have recently demonstrated a surface-sensitive thermometric technique, which is unaffected by mechanical stress, based on the use of diamond microparticles as micro-Raman thermometers for gate temperature measurements.

In this work, we use the diamond micro-Raman thermometer technique proposed by Simon et al. [8] to measure the surface temperature of ungated AlGaN/GaN transistors. We demonstrate that this technique combined with standard micro-Raman thermography measurements can be used to determine the vertical temperature gradient in the GaN layer of an AlGaN/GaN HEMT. Combining these results with thermal modelling enables the thermal conductivity of the GaN layer to be determined.

**2 Experimental details** AlGaN/GaN ungated transistors and single-finger HEMTs with a 30 nm-thick AlN nucleation layer, 1.5 µm-thick carbon-doped GaN layer and 18 nm-thick $Al_{0.25}Ga_{0.75}N$ barrier layer, grown by metal organic chemical vapour deposition (MOCVD) on a 370 µm-thick vanadium-doped 6H-SiC substrate, as shown schematically in Figure 1, were studied. The carbon-doping concentration of the GaN layer and the vanadium-doping concentration of the substrate were both $10^{17}$ $cm^{-3}$. The ungated transistors and HEMTs were fabricated with Ti/Al/Mo/Au (15/60/35/50 nm) ohmic contacts which were annealed at 850 °C for 30 s in $N_2$ and were surface-passivated with 150 nm-thick silicon nitride. The gate contact of the HEMTs was fabricated with standard Schottky gate Ni/Au metallisation. Mesa isolation was achieved by etching to a depth of 170 nm using inductively coupled plasma-reactive ion etching (ICP-RIE). The ungated transistors had a separation of 4 µm between the ohmic contacts, device width of 91 µm and were DC-biased with 13.40 V, 92.17 mA resulting in a power dissipation of 1.24 W. The HEMTs had a gate length of 3.5 µm, a source-drain separation of 26 µm and a device width of 211 µm. They were operated with a source-drain bias of 39.55 V with source-drain current of 47.17 mA and gate voltage of 0 V, (threshold voltage of -2.9 V) giving a power dissipation of 1.87 W.

Micro-Raman thermography was utilized to measure the temperature of the carbon-doped GaN layer in both the ungated transistors and HEMTs using the temperature dependence of the GaN $A_1$(LO) phonon mode, obtaining a temperature accuracy within ~5 °C. The technique was performed using a 532 nm frequency-doubled Nd:YAG laser (3 mW incident power) and a Renishaw InVia spectrometer. Laser light was focused, and scattered light collected, using a 50x 0.5 numerical aperture objective lens, achieving a lateral spatial resolution of 0.5 µm. More details on the micro-Raman thermography technique can be found in [9]. The GaN temperature measured represents a volumetric depth average as GaN is transparent to the wavelength used. This is evident in Figure 1(A) where the laser penetrates through the GaN layer. Micro-Raman thermography mapping was performed using a motorized XYZ translation stage with a 0.1 µm step resolution. For the ungated transistor, lateral maps were recorded from the centre of the channel between contacts to 55 µm outside the active device area beyond the mesa edge, illustrated in Figure 3. For the HEMT, mapping was performed from drain to source contact along the centre of the device. The wafer backplate temperature was maintained at 25 °C using a thermoelectric chuck.

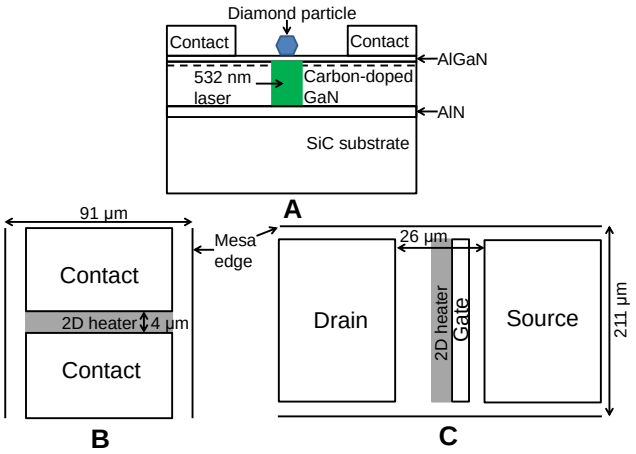


**Figure 1** A) Cross-section of ungated transistor with epilayer structure 18 nm-thick $Al_{0.25}Ga_{0.75}N$ barrier layer/1.5 µm-thick carbon-doped GaN layer/30 nm-thick AlN nucleation layer/370 µm-thick 6H-SiC substrate with diamond particle on channel between contacts and area averaged in the GaN layer measurement. B) Plan view of ungated transistor with 2D heater between contacts and C) Plane view of HEMT with 2D heater along drain edge of the gate contact, used in thermal modelling.

A suspension of <1 µm diamond particles in ethanol was spray-deposited over the whole ungated transistor area. Five of the deposited diamond particles were measured, at positions shown schematically and graphically in Figure 3. Micro-Raman thermography was employed to measure the temperature of the diamond particles, utilising the temperature dependence of the diamond 1332 $cm^{-1}$ phonon line. In previous work, the diamond particle was seen to reach thermal equilibrium with the gate contact after 10 µs [8]. Therefore in the DC steady-state measurements performed here, the diamond particle is in thermal equilibrium with the device surface. There will be negligible heat flow from the transistor channel through the AlGaN barrier layer and SiN passivation layer to the diamond particle and hence a negligible temperature gradient and thermal resistance between the particle and device surface.

A three-dimensional (3D) finite element thermal model, was constructed in ANSYS®[10]. For comparison to the

experimental results, the surface temperature of and depth-averaged GaN temperature, corresponding to the diamond particle and GaN layer Raman measurements, respectively, were simulated. A quarter of the ungated transistor was modelled due to the symmetry in the device layout. A uniform power dissipation was applied in the model, implemented as a uniform 2D heat source at the AlGaN/GaN interface, between contacts, representing the uniform Joule heating resulting from the in-plane electric field [11]. This region is highlighted in Figure 1(B). Three fitting parameters were implemented in the model; the GaN buffer thermal conductivity, the AlN nucleation layer thermal resistance and the SiC substrate thermal conductivity, adjusted to best fit the measured temperatures. Similarly, a 3D-finite element thermal model of half of the HEMT was constructed. Due to the highest electric field region being present in a HEMT along the drain edge of the gate [12], a uniform 2D heat source was placed here, as shown in Figure 1(C), and the length of this heater was adjusted to best fit the simulation to the experimental temperature results.

**3 Results and discussion** In order to determine the SiC substrate thermal conductivity, the average temperature of the GaN layer was measured laterally outside the active device region beyond the mesa edge of the ungated transistor, as shown schematically in the inset of Figure 2. In this region the substrate thermal conductivity determines the GaN temperature, whereas inside the active device area, there are additional contributions from the GaN layer itself and the AlN nucleation layer [13].

The best fit of the simulated average GaN temperature profile to the experimental data, illustrated in Figure 2, was achieved with a thermal conductivity of 330 $Wm^{-1}K^{-1}$ for the SiC substrate in the thermal model, including a temperature dependence of $T^{-1.5}$ [9]. The thermal conductivity obtained is consistent with reported values for vanadium doped SiC [14]. This value was used for all subsequent thermal simulations.

Figure 3 shows the measured (depth average) GaN temperature profile across the ungated transistor, from the centre of the device channel to 55 µm outside the active device area (outside the mesa edge) along with the temperature of five diamond particles (1-5) deposited on the ungated transistor channel area, at positions shown schematically in the inset. As mentioned previously these diamond particle temperatures correspond to the GaN surface temperature underneath the particles. Fitting the thermal simulation to the GaN layer average and surface temperature (vertical temperature gradient), shown by the solid line and dashed line respectively, yielded a thermal conductivity of 200 $Wm^{-1}K^{-1}$ for the 1.5 µm-thick carbon-doped GaN layer, including a temperature dependence of $T^{-1.4}$ [9] It should be noted that diamond particles 3 and 4 were not used in the fitting process due to their position close to the edge of the device and between contact edge and mesa edge respectively, which are not well defined, resulting in the discrepency observed between these diamond particle temperatures and simulation. The shaded regions above and below the best fit simulation illustrates a ±10 % (±20 $Wm^{-1}K^{-1}$) range of GaN thermal conductivity around the best fit value. The temperature gradient across the AlN nucleation layer was significantly smaller than the temperature gradient across the GaN layer and therefore the simulation result was not sensitive to the thermal boundary resistance parameter in this case.

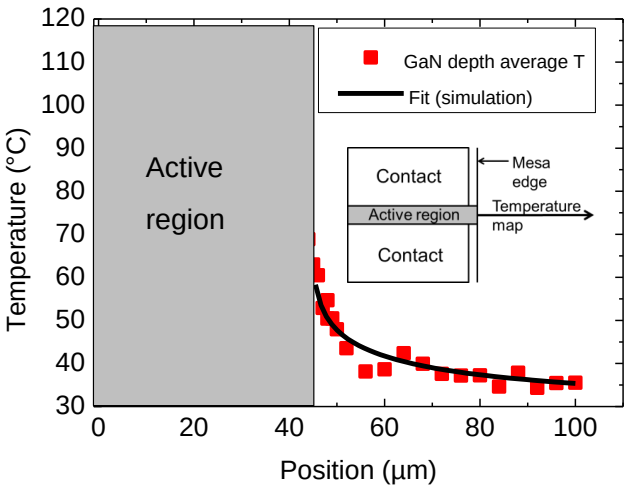


**Figure 2** Experimentally-measured lateral GaN layer T (temperature) profile and (the linescan shown schematically in the inset). The best fit simulation result using a thermal conductivity of 330 $Wm^{-1}K^{-1}$ for the SiC substrate is overlaid.

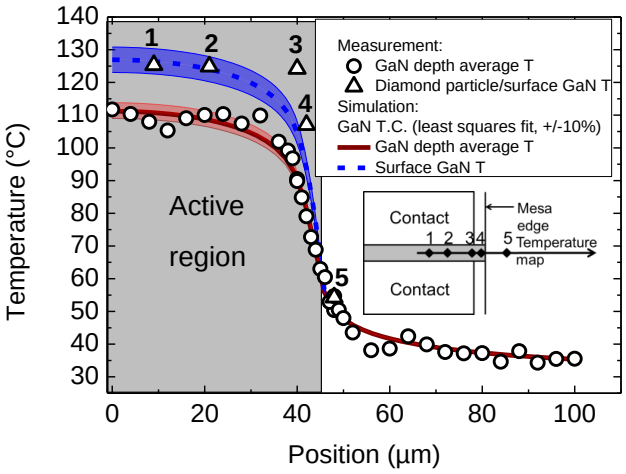


**Figure 3** Experimentally-determined depth average GaN temperature profile and surface GaN temperature with diamond particles 1-5. The simulation result with the best fit GaN thermal conductivity of 200 $Wm^{-1}K^{-1}$ and +/-10 % range (shaded region) are overlaid.

The thermal conductivity value obtained for the carbon-doped GaN layer is in the range of previously reported

values; 185±20 $Wm^{-1}K^{-1}$ and 186-210 $Wm^{-1}K^{-1}$, measured by time-domain thermoreflectance (TDTR) [15] and scanning thermal microscopy (SThM) [16], respectively. The advantage of the technique presented here is that a standard device wafer can be used, without the need for any special preparation.

To verify the GaN thermal conductivity obtained, GaN average temperature profiles between drain and source of a HEMT were measured and compared to simulation (using the previously determined thermal conductivity value of 200±20 $Wm^{-1}K^{-1}$ for the carbon-doped GaN buffer layer) as shown in Figure 4. The epilayer structure of the HEMT is the same as that of the ungated transistor studied in this work.

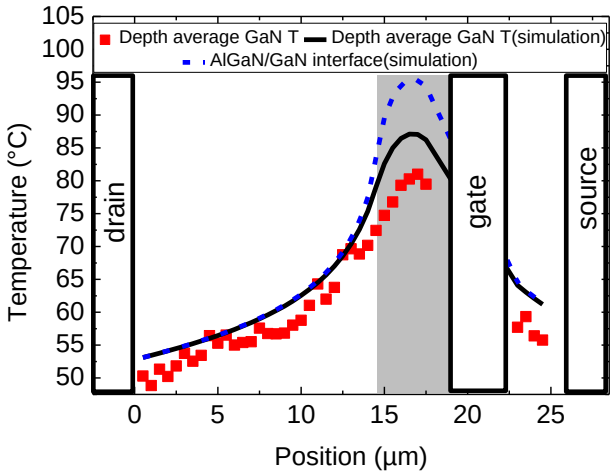


**Figure 4** Experimentally-determined GaN layer depth average temperature profile and simulated GaN depth average and AlGaN/GaN interface temperature profiles from drain to source in an AlGaN/GaN HEMT using GaN layer thermal conductivity of 200 $Wm^{-1}K^{-1}$ and 2D heater length of 4.5 µm. The shaded region represents the 2D heater used in the thermal model.

It can be seen that the highest temperature is located near the drain edge of the gate contact as expected. The simulated GaN average temperature profile from drain to source contact fits the experimental data quite well when a heater length of 4.5 µm is used. This agreement verifies the thermal conductivity of the carbon-doped GaN layer obtained from the ungated transistor measurement. The extension of the high electric field region away from the gate edge indicates the presence of a virtual gate [12], and in that case it is important to note that the assumed block heat load at the HEMT gate edge is a simplification of the real electric field profile. Nevertheless, there is reasonably good agreement between measurement and simulation, as previously noted. For comparison, the simulated peak channel temperature at the AlGaN/GaN interface is also shown in Figure 4, which depends strongly on the GaN thermal conductivity used in the thermal model, again, highlighting the importance of verifying the GaN buffer layer thermal conductivity.

**4 Conclusion** By combining a diamond micro-thermometer technique in combination with standard Raman thermography, a thermal conductivity of 200±20 $Wm^{-1}K^{-1}$ has been determined for a carbon-doped GaN buffer layer with a doping concentration of $10^{17}$ $cm^{-3}$. This result was verified by comparing the results of a HEMT thermal model including the GaN thermal conductivity obtained to micro-Raman thermography measurement.

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